PATENT APPLICATION
DOCKET NO.: 10010788-1

REMARKS

Claims 1-29 are currently pending. Claims 1, 11, and 21 are in independent form.

Claims 1, 11, and 21 have been amended. No new matter is introduced hereby.

Favorable reconsideration of the present application as currently constituted is respectfully requested.

Regarding the Claim Rejections - 35 U.S.C. §103(a)

Part I

Claims 1, 11-14, 19, 20, 22-24, and 28-29 stand rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,516,362 to Magro et al. (hereinafter the *Magro* reference) in view of U.S. Patent Application Publication No. 2002/0009169 to Watanabe (hereinafter the *Watanabe* reference). In connection with these rejections, the instant Office Action includes comments that are at least substantially similar to those provided in the Office Action of September 13, 2004 with respect to the base claims 1 and 11.

Applicant respectfully submits that the foregoing §103(a) claim rejections have been overcome or otherwise rendered moot by way of the present response. The present invention, as defined by the currently-amended base claim 1, is directed to a system for

synchronizing a first circuit portion operating in a first clock domain (clocked with a first clock signal) and a second circuit portion operating in a second clock domain (clocked with a second clock signal). A SYNC pulse signal is generated based on occurrence of a coincident edge between the first and second clock signals. As presently claimed, the SYNC pulse signal comprises a SYNC pulse for every N clock cycles of the first clock signal. A clock synchronizer controller is provided for generating a plurality of control signals based on the SYNC pulse signal, which clock synchronizer controller includes a SYNC adjuster operable to re-position the SYNC pulse signal based on a new coincident edge between the first and second clock signals that is defined in response to a skew between the clock signals.

In a further aspect, the base claim 11 is drawn to a method of synchronizing data transfer operations between two circuit portions across a clock domain boundary. The method embodiment of claim 11 includes, *inter alia*, generating a SYNC pulse signal based on occurrence of a coincident edge between primary and secondary clock signals, wherein the SYNC pulse signal comprises a SYNC pulse for every N clock cycles of the first clock signal, and adjusting the SYNC pulse signal to re-position it based on a new coincident edge that is defined response to a skew between the clock signals.

Similarly, the method embodiment of base claim 21 involves, *inter alia*, generating a SYNC pulse signal based on occurrence of a coincident edge between a primary clock signal operable with a first clock domain and a secondary clock signal operable with a second clock domain, wherein skew compensation is based on (i) determining a state indicative of a phase difference between the primary and secondary clock signals, and (ii) redefining a new coincident edge with respect to the primary and secondary clock signals based on the state. As currently constituted, the SYNC pulse signal comprises a SYNC pulse for every N clock cycles of the first clock signal.

In contrast, the *Magro* reference does not teach or suggest generating a SYNC pulse signal based on occurrence of a coincident edge between two clock signals wherein the SYNC pulse signal comprises a SYNC pulse for every N clock cycles of the first clock signal. Also, it does not teach or suggest a SYNC adjuster operable to re-position the SYNC pulse signal based on a new coincident edge between the two clock signals that is defined in response to a skew between the clock signals. More specifically, the *Magro* reference is directed to a computer system that includes circuits/devices clocked at different clock frequencies and having skewed clock signals. Based on two clock signals, clk_cpu 106 and

clk_mem 108, a synchronization signal called phase_sync signal 206 is generated that is identical to one of the clock signals, see FIG. 3a and FIG. 3b, rather than having a pulse for every N clock cycles. Further, there is absolutely no teaching or even a scintilla of suggestion in the *Magro* reference with respect to adjusting the phase_sync signal 206 in order to re-position it based on a new coincident edge between the clk_mem and clk_cpu signals.

The critical deficiencies of the *Magro* reference as applied to the base claims 1, 11 and 21 are not cured by the secondary reference, i.e., the *Watanabe* reference, when combined as a basis for obviousness in the pending Office Action. It is well known that to establish obviousness, three basic criteria must be met. First, there must be some suggestion or motivation to modify the references or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the combined references must teach or suggest all the claim limitations. See MPEP §2143. Applicant respectfully maintains that there is no suggestion or motivation in either of the applied references to combine the teachings therein so as to achieve the claimed invention directed to a solution where a SYNC adjuster mechanism is provided for re-positioning a SYNC pulse signal based on a new

coincident edge between first and second clock signals that is defined in response to a skew between the clock signals. As pointed out in the foregoing, the *Magro* reference is concerned with skew between two clock signals that are used clocking different parts of a computer system. In contrast, the *Watanabe* reference is concerned with skew between parallel data channels in a data transmission system. Specifically, *Watanabe* discloses a skew correction apparatus for making the deskew work possible even during the transmission of data in a data transmission system (see, e.g., paragraphs [0012] and [0013]), wherein skew amount constitutes a phase difference within different data transmission channels disposed between a transmitter 51 and a receiver 52 (see FIG. 5; see also paragraph [0066]). Applicant respectfully submits that the skew correction apparatus of *Watanabe* is concerned with correcting the skew in the data channels during the idle time when no data is transmitted, as well as with correcting the skew during the data transmission after correcting the skew by the first skew correction means. See paragraph [0013]; see also FIG. 3. To the extent the skew correction means of the *Watanabe* reference is not at all concerned with generating a SYNC pulse based on occurrence of a coincident edge between two clock signals and adjusting the SYNC pulse in order to re-position it based on a new coincident

edge between the clock signals, there would be no motivation to combine the teachings of the *Magro* and *Watanabe* references, as there is little likelihood of success in obtaining an operable result.

Further, to the extent that *Magro* and *Watanabe* references belong to different PTO Classes and to the extent that there exist substantial structural and functional dissimilarities between these two references as explained in the foregoing, it is respectfully asserted that any finding of motivation to combine the references is negatived. See MPEP §2141.01(a). In addition, even if the teachings of the *Magro* and *Watanabe* references were to be combined somehow, it is clear that the combined teachings do not teach or suggest all the claim limitations including, *inter alia*, generating a SYNC pulse signal that comprises a SYNC pulse for every N clock cycles of a clock signal.

Accordingly, Applicant respectfully submits that claims 1, 11-14, 19, 20, 22-24, and 28-29 are patentable over the *Magro* and *Watanabe* references.

Part II

In the pending Office Action, claims 15-17, 21, and 25-26 stand rejected under 35 U.S.C. §103(a) as being unpatentable over

the *Magro* and *Watanabe* references as applied to claim 11 above, and further in view of U.S. Patent No. 6,212,249 to Shin (hereinafter the *Shin* reference).

Applicant respectfully submits that the foregoing §103(a) rejections have been overcome or otherwise rendered moot by way of the present response. As discussed in the foregoing section, the combination of the *Magro* and *Watanabe* references is of no avail in terms of providing a proper basis for the §103(a) rejection of the base claims 11 and 21. Application of the *Shin* reference does not cure this deficiency, however. *Shin* discloses a data separation circuit and method for a floppy disk controller in which the data rate with which the data is read from the floppy disk may increase (i.e., a fast state) or decrease (i.e., a slow state). Col. 5, lines 7 - 17. A window signal (FIG. 3C) is employed that includes a data area and a clock area for dividing read data bits and clock pulses from a common read data stream. Col. 4, line 58 to col. 5, line 6. For proper operation, the window signal must also change as the data rate changes. Col. 5, lines 17 - 21.

As shown in FIG. 2, the data separation circuit of *Shin* includes a digital phase-locked loop (DPLL) 29 that outputs the window signal. Although DPLL 29 operates to increase or decrease the length of time between pulses in the window signal in

accordance with changes in data rate based on a reference clock, it does not generate a separate SYNC pulse based upon occurrence of a coincident edge between the window and reference clock signals. Further, the phase difference states determined by the phase detecting part 25 of the *Shin* reference do not suggest or allude to redefining a new coincident edge between two clock signals based on the determined state. Nor do the phase difference states relate to adjusting a SYNC pulse signal in response thereto.

Applicant respectfully submits that there is no suggestion or motivation in any of the applied references to combine the teachings therein so as to achieve the claimed invention directed to a solution where a SYNC adjuster mechanism is provided for re-positioning a SYNC pulse signal based on a new coincident edge between first and second clock signals that is defined in response to a state indicative of a phase difference. On the other hand, even if the teachings of the *Magro* and *Watanabe* references were to be combined somehow with the teachings of the *Shin* reference, it is respectfully contended that the combined teachings do not teach or suggest all the claim limitations including, *inter alia*, generating a SYNC pulse signal that comprises a SYNC pulse for every N clock cycles of a clock signal. Additionally, is no reasonable expectation of achieving success because of the requirement that

the phase_sync signal of the *Magro* reference be generated only when there is a fixed phase relationship between the two clock signals, which teaches away from variable phase differences in either direction between the reference clock and window signals as disclosed in the *Shin* reference.

Accordingly, Applicant respectfully submits that claims 15-17, 21, and 25-26 are patentable over the *Magro*, *Watanabe* and *Shin* references.

Part III

In the outstanding Office Action, claim 18 and 27 are rejected under 35 U.S.C. §103(a) as being unpatentable over the *Magro* reference (as applied to the base claims 11 and 21 above) in view of U.S. Patent No. 5,987,081 to Csoppenszky et al. (hereinafter the *Csoppenszky* reference). Applicant respectfully submits that these §103(a) rejections have been overcome or otherwise rendered moot by way of the present response. As discussed above with respect to the base claims 11 and 21, the *Magro* reference is deficient when applied as a primary reference. On the other hand, reliance on the *Csoppenszky* reference is of no avail in this regard. The *Csoppenszky* reference is concerned with deterministic transferring of data across an asynchronous boundary in a test environment.

Col. 2, lines 40-42. A synchronizer comprising a series of flip-flops is provided for effectuating data transfer from one clock domain to a second clock domain operating at a higher clock frequency. Col. 2, lines 43-46. A clock enable signal is defined so as to approximately align the enabled rising edges of the faster clock signal with the falling edges of the slower clock signal. This approximate alignment provides a timing window of one half period of the slower clock for the data to stabilize at the input of a flip-flop in the faster clock domain before it is sampled. Col. 2, lines 54-57.

Applicant respectfully contends that there is no suggestion or motivation in either of the applied references to combine the teachings therein so as to achieve the claimed invention wherein a SYNC pulse signal is generated based on occurrence of a coincident edge between two clock signals, which SYNC pulse signal is operable to be adjusted so as to re-position it based on a new coincident edge that is defined responsive to a skew between the two clock signals. In addition, the combination of the *Magro* and *Csoppenszky* references fails to teach or suggest all of the limitations of the present invention as currently claimed. Accordingly, Applicant respectfully submits that claims 18 and 27, which are dependent

from the base claims 11 and 21, respectively, are patentable over the applied combination of the references.

Regarding the Allowable Subject Matter

Applicant gratefully appreciates the indication in the pending Office Action that claims 2-10 "would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims." In view of the present response, it is believed that claims 2-10 are in condition for allowance in their current form.

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SUMMARY AND CONCLUSION

In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the outstanding rejections and allow claims 1-29 presented for reconsideration herein. Accordingly, a favorable action in the form of an early notice of allowance is respectfully requested.

Respectfully submitted,

Dated: 6/3/05

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